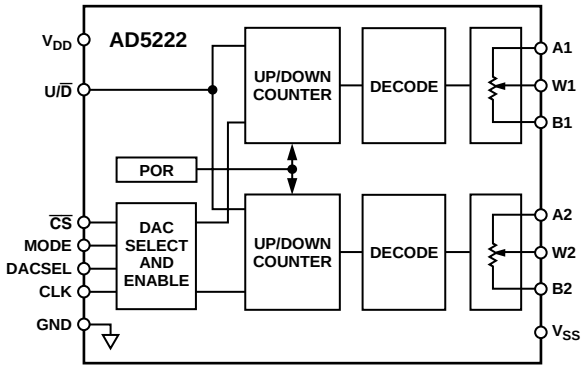
# Increment/Decrement Dual Digital Potentiometer

# AD5222

**FEATURES**
**128-Position, 2-Channel Potentiometer Replacement**
**10 kΩ, 50 kΩ, 100 kΩ, 1 MΩ**
**Very Low Power: 40 μA Max**
**±2.7 V Dual Supply Operation or 2.7 V to 5.5 V Single Supply Operation**
**Increment/Decrement Count Control**

**APPLICATIONS**
**Stereo Channel Audio Level Control**
**Mechanical Potentiometer Replacement**
**Remote Incremental Adjustment Applications**
**Instrumentation: Gain, Offset Adjustment**
**Programmable Voltage-to-Current Conversion**
**Line Impedance Matching**

**FUNCTIONAL BLOCK DIAGRAM**




## GENERAL DESCRIPTION

The AD5222 provides a dual channel, 128-position, digitally controlled variable-resistor (VR) device. This device performs the same electronic adjustment function as a potentiometer or variable resistor. These products were optimized for instrument and test equipment push-button applications. Choices between bandwidth or power dissipation are available as a result of the wide selection of end-to-end terminal resistance values.

The AD5222 contains two fixed resistors with wiper contacts that tap the fixed resistor value at a point determined by a digitally controlled up/down counter. The resistance between the wiper and either end point of the fixed resistor provides a constant resistance step size that is equal to the end-to-end resistance divided by the number of positions (e.g., $R_{STEP}$ = 10 kΩ/128 = 78 Ω). The variable resistor offers a true adjustable value of resistance, between Terminal A and the wiper, or Terminal B and the wiper. The fixed A-to-B terminal resistance of 10 kΩ, 50 kΩ, 100 kΩ, or 1 MΩ has a nominal temperature coefficient of –35 ppm/°C.

The chip select $\overline{CS}$, count CLK and U/$\overline{D}$ direction control inputs set the variable resistor position. The MODE determines whether both VRs are incremented together or independently. With MODE at logic zero, both wipers are incremented UP or DOWN without changing the relative settings between the wipers. Also, the relative ratio between the wipers is preserved if either wiper reaches the end of the resistor array. In the independent MODE (Logic 1) only the VR determined by the DACSEL pin is changed. DACSEL (Logic 0) changes RDAC 1. These inputs, which control the internal up/down counter, can be easily generated with mechanical or push-button switches (or other contact closure devices). This simple digital interface eliminates the need for microcontrollers in front panel interface designs.

The AD5222 is available in the surface-mount (SO-14) package. For ultracompact solutions, selected models are available in the thin TSSOP-14 package. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C. For 3-wire, SPI-compatible interface applications, see the AD5203/AD5204/AD5206, AD7376, and AD8400/AD8402/AD8403 products.

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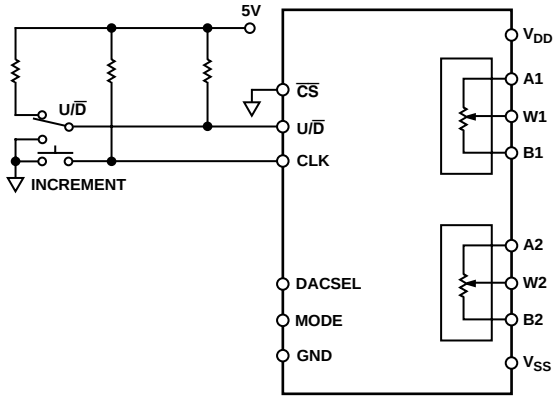


*Figure 1. Typical Push-Button Control Application*

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# AD5222–SPECIFICATIONS ($V_{DD}$ = 3 V ± 10% or 5 V ± 10%, $V_{SS}$ = 0 V, $V_A$ = +$V_{DD}$, $V_B$ = 0 V, –40°C < $T_A$ < +85°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DC CHARACTERISTICS RHEOSTAT MODE (Specifications Apply to All VRs) | | | | | | |
| Resistor Differential NL[2] | R-DNL | $R_{WB}$, $V_A$ = NC | –1 | ±1/4 | +1 | LSB |
| Resistor Nonlinearity[2] | R-INL | $R_{WB}$, $V_A$ = NC | –1 | ±0.4 | +1 | LSB |
| Nominal Resistor Tolerance | ΔR | $V_{AB}$ = $V_{DD}$, Wiper = No Connect, $T_A$ = 25°C | –30 | | +30 | % |
| Resistance Temperature Coefficient | $R_{AB}/\Delta T$ | $V_{AB}$ = $V_{DD}$, Wiper = No Connect | | –35 | | ppm/°C |
| Wiper Resistance[3] | $R_W$ | $I_W$ = $V_{DD}$/R, $V_{DD}$ = 3 V or 5 V | | 45 | 100 | Ω |
| Nominal Resistance Match | $\Delta R/R_O$ | CH 1 to 2, $V_{AB}$ = $V_{DD}$, $T_A$ = 25°C | | 0.2 | 1 | % |
| DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE (Specifications Apply to All VRs) | | | | | | |
| Resolution | N | | 7 | | | Bits |
| Integral Nonlinearity[4] | INL | $R_{AB}$ = 10 kΩ, 50 kΩ, or 100 kΩ | –1 | ±1/4 | +1 | LSB |
| | INL | $R_{AB}$ = 1 MΩ | –2 | ±1/2 | +2 | LSB |
| Differential Nonlinearity[4] | DNL | | –1 | ±1/4 | +1 | LSB |
| Voltage Divider Temperature Coefficient | $\Delta V_W/\Delta T$ | Code = $40_H$ | | 20 | | ppm/°C |
| Full-Scale Error | $V_{WFSE}$ | Code = $7F_H$ | –1 | –0.5 | +0 | LSB |
| Zero-Scale Error | $V_{WZSE}$ | Code = $00_H$ | 0 | 0.5 | 1 | LSB |
| RESISTOR TERMINALS | | | | | | |
| Voltage Range[5] | $V_{A, B, W}$ | | $V_{SS}$ | | $V_{DD}$ | V |
| Capacitance[6] A, B | $C_{A, B}$ | f = 1 MHz, Measured to GND, Code = $40_H$ | | 45 | | pF |
| Capacitance[6] W | $C_W$ | f = 1 MHz, Measured to GND, Code = $40_H$ | | 60 | | pF |
| Common-Mode Leakage | $I_{CM}$ | $V_A$ = $V_B$ = $V_W$ | | 1 | | nA |
| DIGITAL INPUTS AND OUTPUTS | | | | | | |
| Input Logic High | $V_{IH}$ | $V_{DD}$ = 5 V/3 V | 2.4/2.1 | | | V |
| Input Logic Low | $V_{IL}$ | $V_{DD}$ = 5 V/3 V | | | 0.8/0.6 | V |
| Input Current | $I_{IL}$ | $V_{IN}$ = 0 V or 5 V | | | ±1 | μA |
| Input Capacitance[6] | $C_{IL}$ | | | 5 | | pF |
| POWER SUPPLIES | | | | | | |
| Power Single-Supply Range | $V_{DD\ RANGE}$ | $V_{SS}$ = 0 V | 2.7 | | 5.5 | V |
| Power Dual-Supply Range | $V_{DD/SS\ RANGE}$ | | ±2.3 | | ±2.7 | V |
| Positive Supply Current | $I_{DD}$ | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V | | 15 | 40 | μA |
| Negative Supply Current | $I_{SS}$ | $V_{SS}$ = –2.5 V, $V_{DD}$ = +2.7 V | | 15 | 40 | μA |
| Power Dissipation[7] | $P_{DISS}$ | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V, $V_{DD}$ = 5 V | | 150 | 400 | μW |
| Power Supply Sensitivity | PSS | | | 0.002 | 0.05 | %/% |
| DYNAMIC CHARACTERISTICS[6, 8, 9] | | | | | | |
| Bandwidth –3 dB | BW_10K | $R_{AB}$ = 10 kΩ, Code = $40_H$ | | 1000 | | kHz |
| | BW_50K | $R_{AB}$ = 50 kΩ, Code = $40_H$ | | 180 | | kHz |
| | BW_100K | $R_{AB}$ = 100 kΩ, Code = $40_H$ | | 78 | | kHz |
| | BW_1M | $R_{AB}$ = 500 kΩ, Code = $40_H$ | | 7 | | kHz |
| Total Harmonic Distortion | $THD_W$ | $V_A$ = 1 V rms + 2 V dc, $V_B$ = 2 V dc, f = 1 kHz | | 0.005 | | % |
| $V_W$ Settling Time | $t_S$ | $R_{AB}$ = 10 kΩ, ±1 LSB Error Band | | 2 | | μs |
| Resistor Noise Voltage | $e_{N_WB}$ | $R_{WB}$ = 5 kΩ, f = 1 kHz | | 14 | | nV√Hz |
| INTERFACE TIMING CHARACTERISTICS (Applies to All Parts)[6, 10] | | | | | | |
| Input Clock Pulsewidth | $t_{CH}$, $t_{CL}$ | Clock Level High or Low | 30 | | | ns |
| $\overline{CS}$ to CLK Setup Time | $t_{CSS}$ | | 20 | | | ns |
| $\overline{CS}$ Rise to CLK Hold Time | $t_{CSH}$ | | 20 | | | ns |
| U/$\overline{D}$ to Clock Fall Setup Time | $t_{UDS}$ | | 10 | | | ns |
| U/$\overline{D}$ to Clock Fall Hold Time | $t_{UDH}$ | | 30 | | | ns |
| DACSEL to Clock Fall Setup Time | $t_{DSS}$ | | 20 | | | ns |
| DACSEL to Clock Fall Hold Time | $t_{DSH}$ | | 30 | | | ns |
| MODE to Clock Fall Setup Time | $t_{MDS}$ | | 20 | | | ns |
| MODE to Clock Fall Hold Time | $t_{MDH}$ | | 40 | | | ns |

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NOTES

[1]Typicals represent average readings at 25°C, $V_{DD}$ = 5 V.

[2]Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Figure 22 test circuit.

[3]Wiper resistance is not measured on the $R_{AB}$ = 1 MΩ models.

[4]INL and DNL are measured at $V_W$ with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A$ = $V_{DD}$ and $V_B$ = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions. See Figure 21 test circuit.

[5]Resistor Terminals A, B, W have no limitations on polarity with respect to each other.

[6]Guaranteed by design and not subject to production test.

[7]$P_{DISS}$ is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

[8]Bandwidth, noise and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

[9]All dynamic characteristics use $V_{DD}$ = 5 V.

[10]See timing diagram for location of measured values. All input control voltages are specified with $t_R$ = $t_F$ = 2.5 ns (10% to 90% of +3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both $V_{DD}$ = 5 V or $V_{DD}$ = 3 V.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS

($T_A$ = 25°C, unless otherwise noted)

$V_{DD}$ to GND . . . . . –0.3 V, +7 V
$V_{SS}$ to GND . . . . . 0 V, –5 V
$V_{DD}$ to $V_{SS}$ . . . . . 7 V
$V_A$, $V_B$, $V_W$ to GND . . . . . 0 V, $V_{DD}$
$A_X – B_X$, $A_X – W_X$, $B_X – W_X$ . . . . . ±20 mA
Digital Input Voltage to GND . . . . . 0 V, $V_{DD}$ + 0.3 V
Operating Temperature Range . . . . . –40°C to +85°C
Maximum Junction Temperature ($T_J$ max) . . . . . 150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Package Power Dissipation . . . . . $(T_J \text{ max} – T_A)/\theta_{JA}$
Thermal Resistance $\theta_{JA}$,
SOIC (SO-14) . . . . . 158°C/W
TSSOP-14 . . . . . 206°C/W

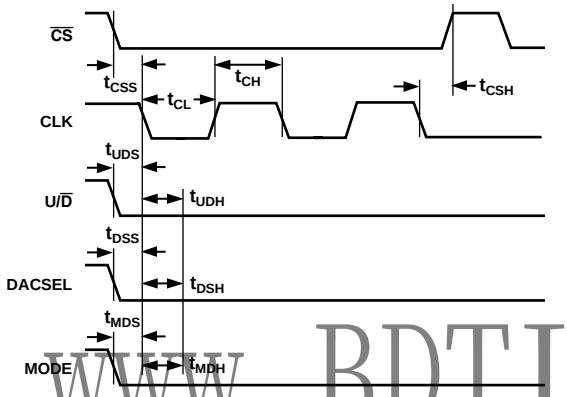


*Figure 2. Detail Timing Diagram*

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**Truth Table**

| $\overline{CS}$ | CLK | U/$\overline{D}$ | Operation |
|---|---|---|---|
| L | ↓ | H | Wiper Increment Toward Terminal A |
| L | ↓ | L | Wiper Decrement Toward Terminal B |
| H | X | X | Wiper Position Fixed |

Common Mode (MODE = 0) moves both wipers together either UP or DOWN the resistor array without changing the relative distance between the wipers. Also, the distance between both wipers is preserved if either reaches the end of the array. Independent Mode (MODE = 1) allows user to control each RDAC individually: DACSEL = 0 sets RDAC1; DACSEL = 1: sets RDAC2.

## ORDERING GUIDE

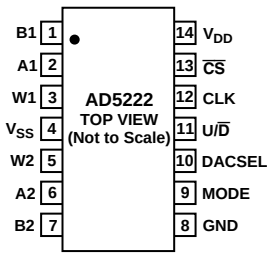
| Model | Kilo Ohms | Temperature | Package Description | Package Option |
|---|---|---|---|---|
| AD5222BR10 | 10 | –40°C/+85°C | SO-14 | R-14 |
| AD5222BRU10 | 10 | –40°C/+85°C | TSSOP-14 | RU-14 |
| AD5222BR50 | 50 | –40°C/+85°C | SO-14 | R-14 |
| AD5222BRU50 | 50 | –40°C/+85°C | TSSOP-14 | RU-14 |
| AD5222BR100 | 100 | –40°C/+85°C | SO-14 | R-14 |
| AD5222BRU100 | 100 | –40°C/+85°C | TSSOP-14 | RU-14 |
| AD5222BR1M | 1,000 | –40°C/+85°C | SO-14 | R-14 |
| AD5222BRU1M | 1,000 | –40°C/+85°C | TSSOP-14 | RU-14 |

The AD5222 die size is 56 mil × 60 mil, 3360 sq. mil; 1.4224 mm × 1.524 mm, 2.1677 sq. mm. Contains 1503 transistors. Patent Number 5495245 applies.

## PIN FUNCTION DESCRIPTIONS

| Pin | Name | Description |
|---|---|---|
| 1 | B1 | B Terminal RDAC #1. |
| 2 | A1 | A Terminal RDAC #1. |
| 3 | W1 | Wiper RDAC #1, DACSEL = 0. |
| 4 | $V_{SS}$ | Negative Power Supply. Specified for operation at both 0 V or –2.7 V (Sum of $\|V_{DD}\| + \|V_{SS}\| < 5.5$ V). |
| 5 | W2 | Wiper RDAC #2, DACSEL = 1. |
| 6 | A2 | A Terminal RDAC #2. |
| 7 | B2 | B Terminal RDAC #2. |
| 8 | GND | Ground. |
| 9 | MODE | Common MODE = 0, Independent MODE = 1. |
| 10 | DACSEL | DAC Select determines which wiper is incremented in the Independent MODE = 1. DACSEL = 0 sets RDAC1, DACSEL = 1 sets RDAC2. |
| 11 | U/$\overline{D}$ | UP/DOWN Direction Control. |
| 12 | CLK | Serial Clock Input, Negative Edge Triggered. |
| 13 | $\overline{CS}$ | Chip Select Input, Active Low. When $\overline{CS}$ is high, the UP/DOWN counter is disabled. |
| 14 | $V_{DD}$ | Positive Power Supply. Specified for operation at both +3 V or +5 V. (Sum of $\|V_{DD}\| + \|V_{SS}\| < 5.5$ V). |

## PIN CONFIGURATION




**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5222 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# AD5222–Typical Performance Characteristics

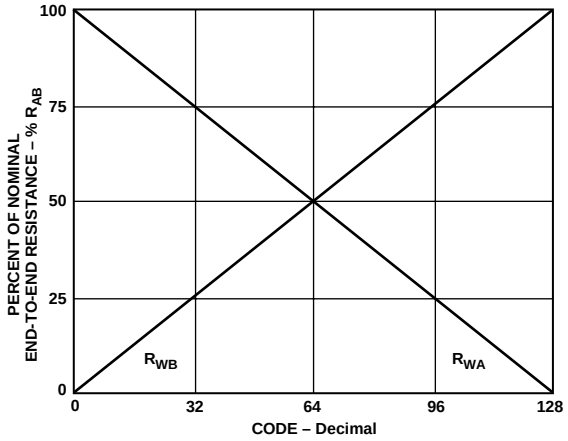



*Figure 3. Wiper-To-End Terminal Resistance vs. Code*

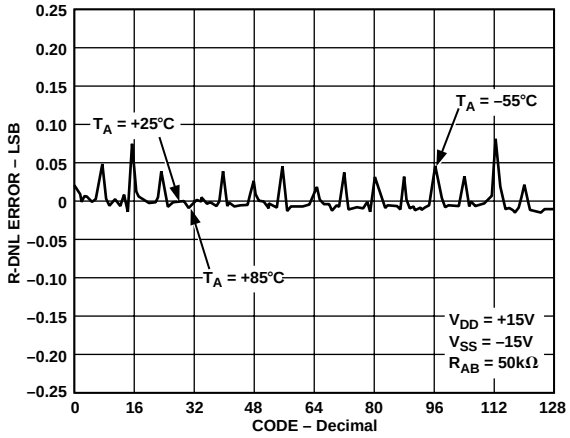



*Figure 6. R-DNL Relative Resistance Step Position Change vs. Code*

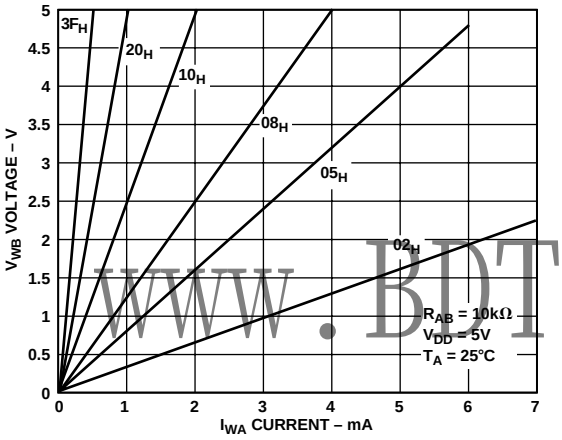



*Figure 4. Resistance Linearity vs. Conduction Current*

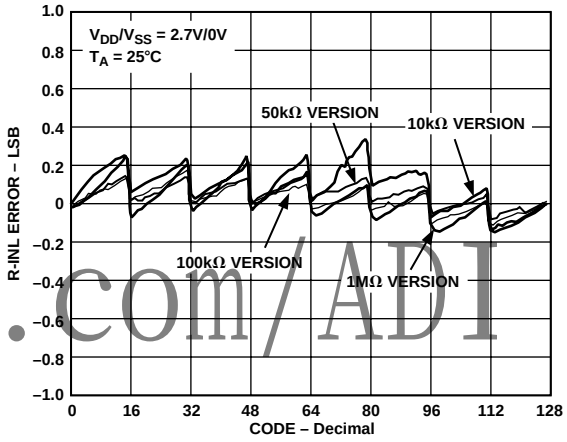



*Figure 7. R-INL Resistance Nonlinearity Error vs. Code*

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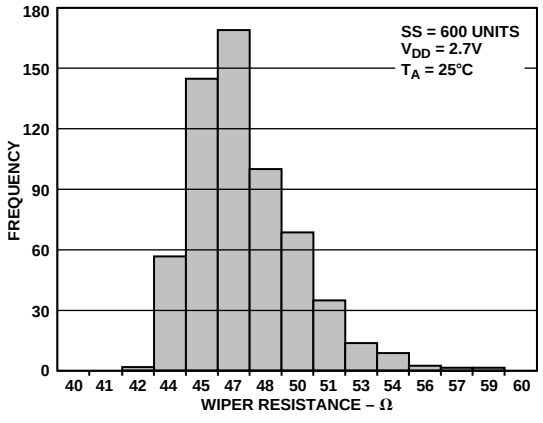


*Figure 5. Wiper Contact Resistance*

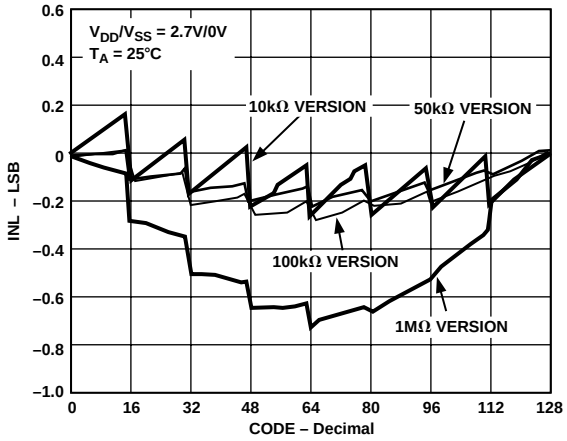


*Figure 8. Potentiometer Divider INL Error vs. Code*

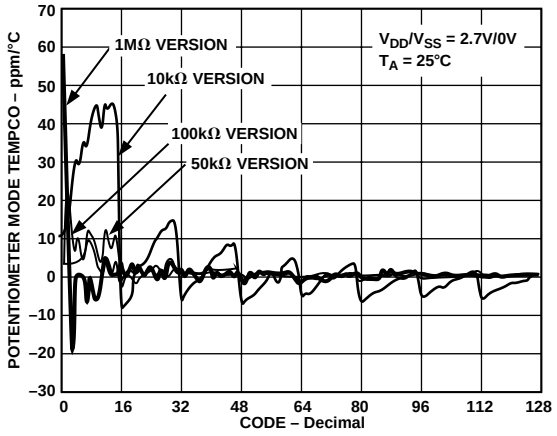


Figure 9. $\Delta V_{WB}/\Delta T$ Potentiometer Mode Tempco

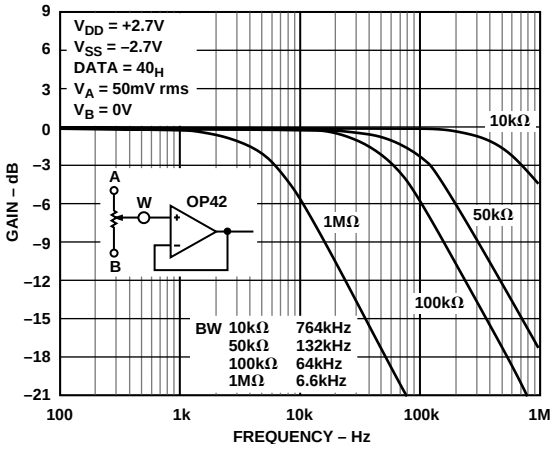


Figure 12. Gain vs. Frequency vs. $R_{AB}$

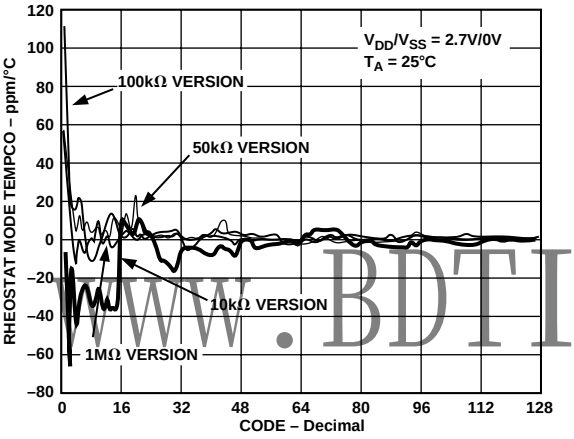


Figure 10. $\Delta R_{WB}/\Delta T$ Rheostat Mode Tempco

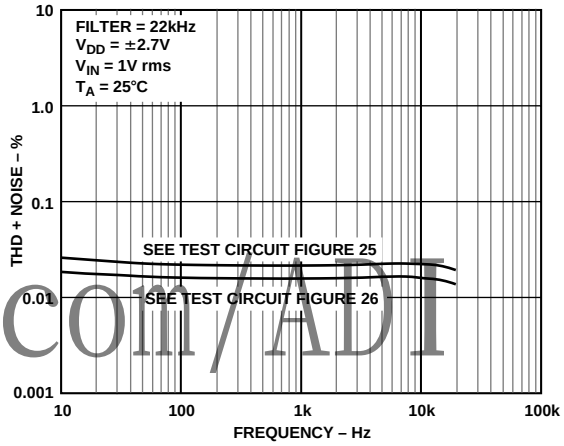


Figure 13. Total Harmonic Distortion Plus Noise vs. Frequency

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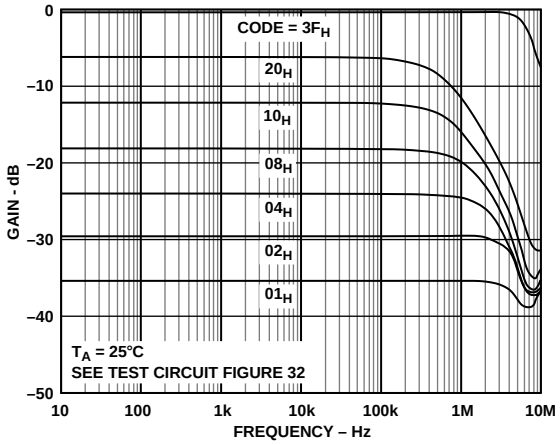


Figure 11. 10 kΩ Gain vs. Frequency vs. Code

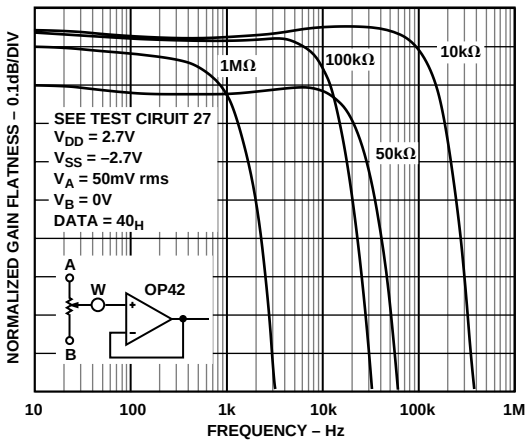


Figure 14. Normalized Gain Flatness vs. Frequency

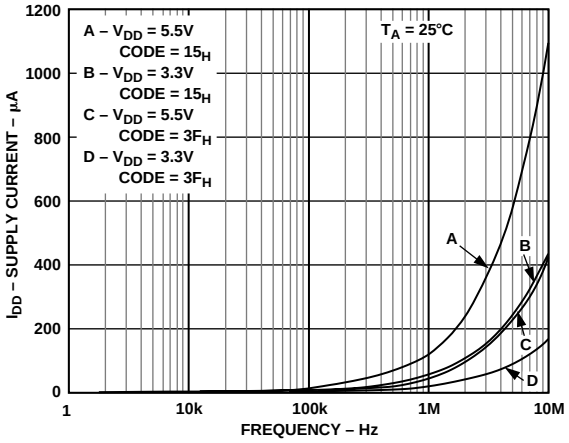


*Figure 15. $I_{DD}$, $I_{SS}$ Supply Current vs. Clock Frequency*

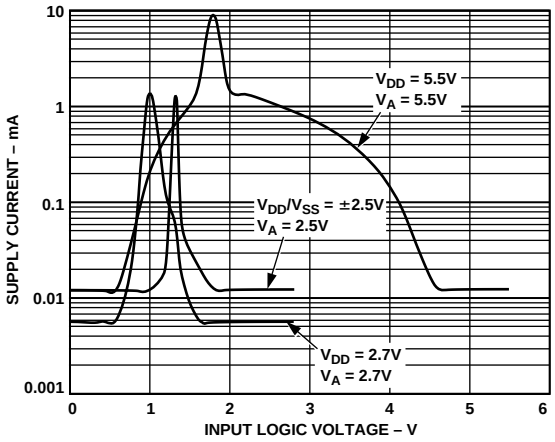


*Figure 18. Supply Current vs. Input Logic Voltage*

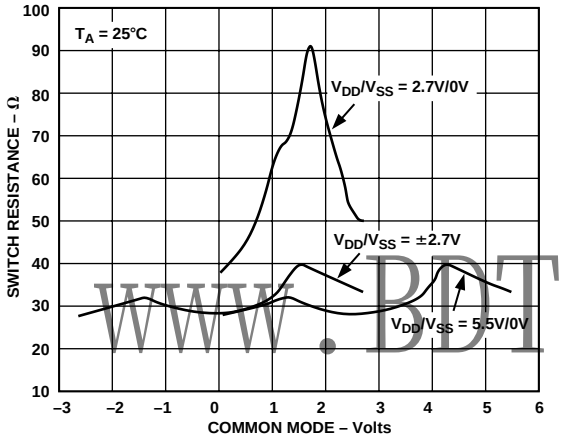


*Figure 16. Incremental Wiper Contact Resistance vs. $V_{DD}/V_{SS}$*

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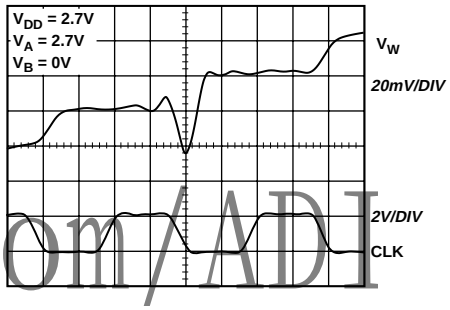


*Figure 19. Midscale Transition $3F_H$ to $40_H$*

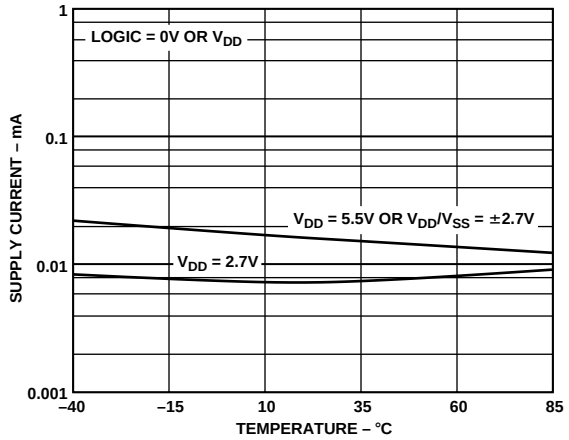


*Figure 17. Supply Current vs. Temperature*

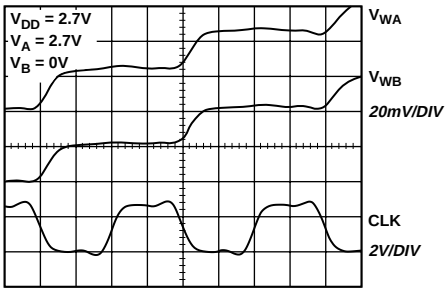


*Figure 20. Stereo Step Transition, Mode = 0*

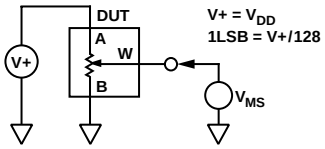


*Figure 21. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)*

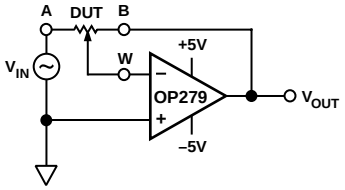


*Figure 25. Inverting Programmable Gain Test Circuit*

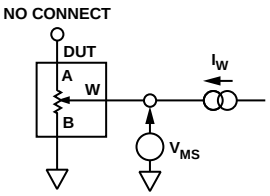


*Figure 22. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)*

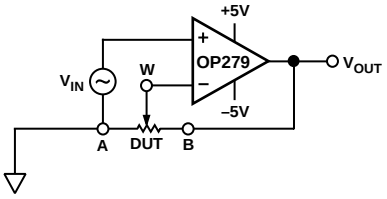


*Figure 26. Noninverting Programmable Gain Test Circuit*

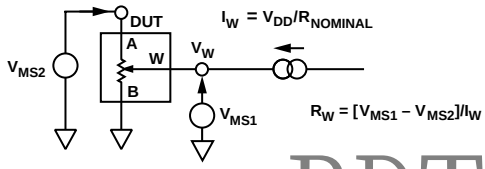


*Figure 23. Wiper Resistance Test Circuit*

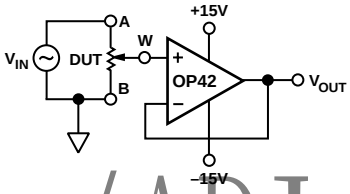


*Figure 27. Gain vs. Frequency Test Circuit*

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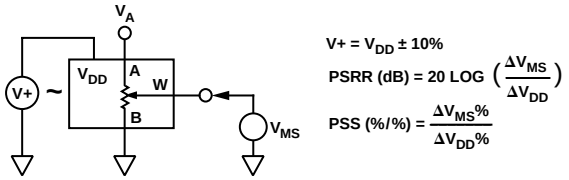


*Figure 24. Power Supply Sensitivity Test Circuit (PSS, PSRR)*

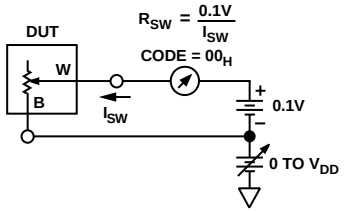


*Figure 28. Incremental ON Resistance Test Circuit*

## OPERATION

The AD5222 provides a 128-position, digitally-controlled, variable resistor (VR) device. Changing the VR settings is accomplished by pulsing the CLK pin while $\overline{CS}$ is active low. The U/$\overline{D}$ (UP/DOWN) control input pin controls the direction of the increment. When the wiper hits the end of the resistor (Terminal A or B) additional CLK pulses no longer change the wiper setting. The wiper position is immediately decoded by the wiper decode logic changing the wiper resistance. Appropriate debounce circuitry is required when push-button switches are used to control the count sequence and direction of count. The exact timing requirements are shown in Figure 2. The AD5222 powers ON in a centered wiper position, exhibiting nearly equal resistances of $R_{WA}$ and $R_{WB}$.

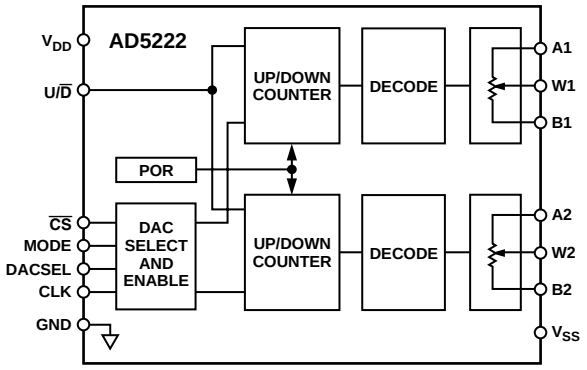


*Figure 29. Block Diagram*

## DIGITAL INTERFACING OPERATION

The AD5222 contains a push-button controllable interface. The active inputs are clock (CLK), $\overline{CS}$ and up/down (U/$\overline{D}$). While the MODE, and DACSEL pins control common updates or individual updates. The negative-edge sensitive CLK input requires clean transitions to avoid clocking multiple pulses into the internal UP/DOWN counter register, Figure 30. Standard logic families work well. If mechanical switches are used for product evaluation a flip-flop or other suitable means should debounce them. When $\overline{CS}$ is taken active low, the clock begins to increment or decrement the internal up/down counter, dependent upon the state of the U/$\overline{D}$ control pin. The UP/DOWN counter value (D) starts at $40_H$ at system power ON. Each new CLK pulse will increment the value of the internal counter by 1 LSB until the full-scale value of $7F_H$ is reached, as long as the U/$\overline{D}$ pin is logic high. If the U/$\overline{D}$ pin is taken to logic low, the counter will count down, stopping at code $00_H$ (zero-scale). Additional clock pulses on the CLK pin are ignored when the wiper is at either the $00_H$ position or the $7F_H$ position. The detailed digital logic interface circuitry is shown in Figure 30.

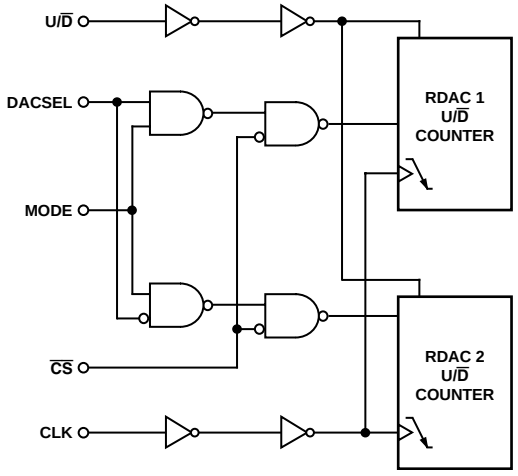


*Figure 30. Detailed Digital Logic Interface Circuit*

All digital inputs ($\overline{CS}$, U/$\overline{D}$, CLK, MODE, DACSEL) are protected with a series input resistor and parallel Zener ESD structure shown in Figure 31. All potentiometer terminal pins (A, B, W) are protected from ESD as shown in Figure 32.

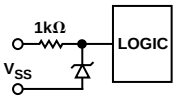


*Figure 31. Equivalent ESD Protection Digital Pins*

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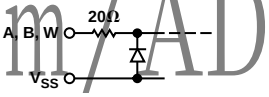


*Figure 32. Equivalent ESD Protection Analog Pins*

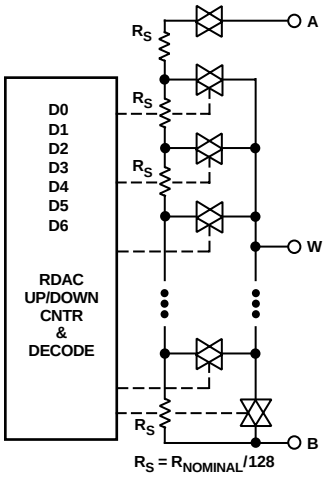


*Figure 33. AD5222 Equivalent RDAC Circuit*

## PROGRAMMING THE VARIABLE RESISTOR

### Rheostat Operation

The nominal resistance of the RDAC between Terminals A and B are available with values of 10 kΩ, 50 kΩ, 100 kΩ, and 1 MΩ The final three characters of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 50 kΩ = 50; 100 kΩ = 100; 1 MΩ = 1M. The nominal resistance ($R_{AB}$) of the VR has 128 contact points accessed by the wiper terminal, plus the B terminal contact. At power ON, the resistance from the wiper to either end Terminal A or B is approximately equal. Pulsing the CLK pin will increase the resistance from the wiper W to Terminal B by one unit of $R_S$ resistance, see Figure 33. The resistance $R_{WB}$ is determined by the number of pulses applied to the clock pin. Each segment of the internal resistor string has a nominal resistance value of $R_S = R_{AB}/128$, which becomes 78 Ω in the case of the 10 kΩ AD5222BR10 product. Care should be taken to limit the current flow between W and B in the direct contact state ($R_{WB}$ code = 0) to a maximum value of 20 mA to avoid degradation or possible destruction of the internal switch contact.

Like the mechanical potentiometer the RDAC replaces, it is totally symmetrical (see Figure 3). The resistance between the wiper W and Terminal A also produces a digitally controlled resistance $R_{WA}$. When these terminals are used the B-terminal should be tied to the wiper.

The typical part-to-part distribution of $R_{BA}$ is process-lot-dependent having a ±30% variation. The change in $R_{BA}$ with temperature has a –35 ppm/°C temperature coefficient.

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The $R_{BA}$ temperature coefficient increases as the wiper is programmed near the B-terminal due to the larger percentage contribution of the wiper contact switch resistance, which has a 0.5%/°C temperature coefficient. Figures 9 and 10 show the effect of the wiper contact resistance as a function of code setting.

## PROGRAMMING THE POTENTIOMETER DIVIDER

### Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal. For example connecting A-terminal to 5 V and B-terminal to ground produces an output voltage at the wiper which can be any value starting at zero volts up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminals AB divided by the 128-position resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to Terminals AB is:

$$V_W(D) = D/128 \times V_{AB} + V_B \quad (1)$$

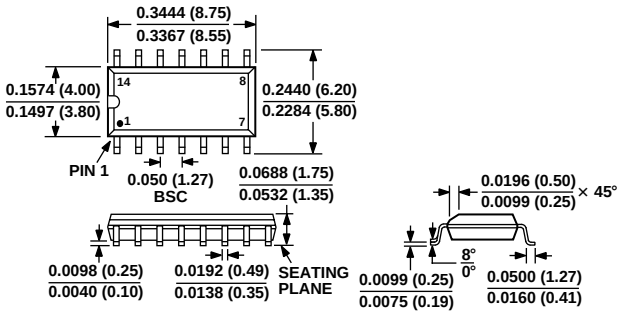
$D$ represents the current contents of the internal up/down counter.

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors not the absolute value, therefore, the drift improves to 20 ppm/°C.

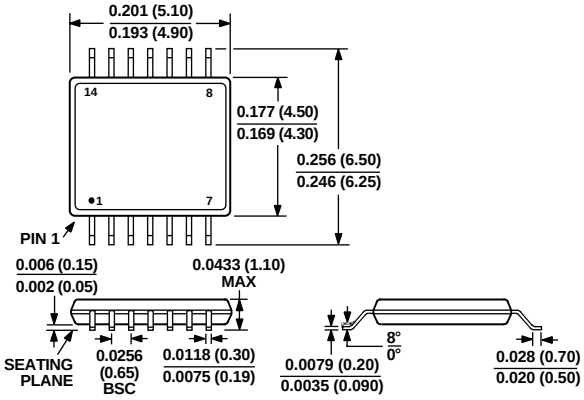
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 14-Lead Narrow Body SOIC (R-14)




### 14-Lead TSSOP (RU-14)

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C3715–8–10/99

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